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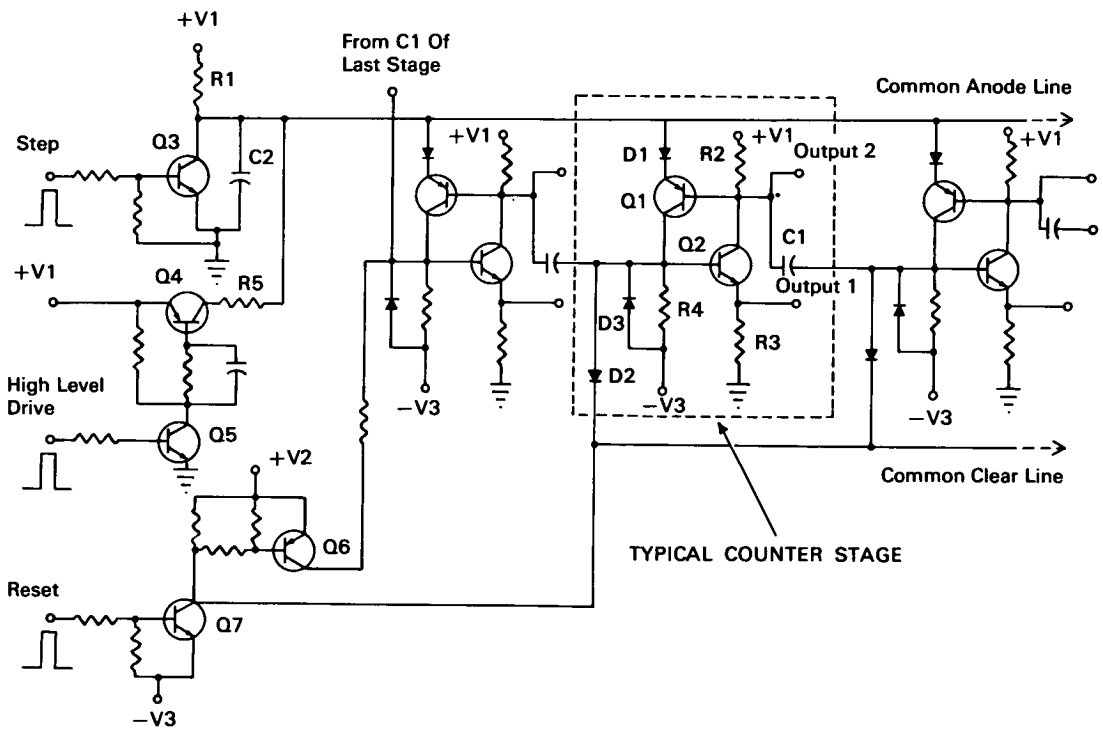
NASA TECH BRIEF

Low-Power Ring Counter Drives High-Level Loads



The problem:

To design a ring counter which dissipates very low power in standby conditions, yet drives high-current loads on a low duty-factor basis.

The solution:

A counter using complementary transistors so that in one selected stage both transistors are conducting, while the transistors of the other stages are cut off. The two transistors in the selected stage carry a very low holding current, and standby dissipation is small. When high-level drive capabilities are required, the holding current is augmented by a pulse of higher current without changing the state of the counter.

How it's done:

In a typical counter stage, transistors Q1 and Q2 form a variation of a silicon-controlled switch. Once the transistors have been turned on by a pulse of current into the base of Q2, they will remain saturated as long as current is flowing through the emitter of Q1. When this holding current is removed, both transistors turn off. While the stage is on, the amplitude of this holding current may be varied over a very wide range without changing the state of the transistors.

(continued overleaf)

A ring counter is made of a number of interconnected stages. By capacitively coupling the output of one stage to the input of the next, the positive-going wavefront of a stage turning off serves to turn on the following one. Counter operation is initiated by pulsing the reset circuit, which turns on the first stage and turns off any other stage which may be on. Holding current then flows through R1 and the common anode line into the first stage. The counter is stepped by momentarily turning on Q3, thus shunting the holding current and causing the first stage to turn off and the second to turn on.

Two types of high-current load may be driven from the counter stage. The first load, connected to output 1, accepts current. The second, connected to output 2, supplies current. Drive capability for both types is provided by pulsing the high-level drive circuit to supplement the holding current to the extent required by the load. Since this high-level capability is required for very short times, the average dissipation is low. Output 1 is intended for driving directly the base of an NPN transistor whose emitter is grounded. If a high-impedance load is connected to that point, the voltage step developed across it during a high-level interval would also appear at the collector of Q2 and might, when coupled through C1, be sufficient to turn on the following stage. When output 1 is not used, R3 should be omitted, and the emitter of Q2 grounded.

Notes:

1. A ring counter requires one stage per count, in contrast to a binary counter in which n stages provide a count of 2^n. In order to cut down on the number of ring counter stages required to achieve a high count, it is possible to use two-dimensional matrix selection. In this technique, two ring counters are used, with the product of the numbers of their stages equaling the required count. The counters are arranged so that each time one counter steps through all its stages, the second counter is stepped once. Thus, by the time the second counter has stepped through all of its stages, the number of distinct combinations achieved is equal to the product of the counters' stages.
2. Inquiries concerning this invention may be directed to:

   Technology Utilization Officer
   Goddard Space Flight Center
   Greenbelt, Maryland, 20771
   Reference: B66-10106

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C., 20546.

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